

**APPENDIX B**  
**VERSION WITH MARKINGS TO SHOW CHANGES MADE**  
**37 C.F.R. § 1.121(b)(iii) AND (c)(ii)**

**CLAIMS:**

4. (Amended) A power MOSFET comprising, in combination[;], a P type substrate;  
an epitaxially deposited N type layer deposited atop said substrate and having a substantially  
constant concentration; a plurality of spaced trenches having vertical walls extending through  
said epitaxial layer; a thin gate oxide on said vertical walls and conductive P type polysilicon  
deposited into said trenches to define a polysilicon gate; a P type source region formed adjacent  
the walls of each of said trenches and diffused into the top of said epitaxial layer; a source  
contact connected to at least said source regions; a drain contact connected to said substrate;  
whereby said MOSFET has a reduced on resistance.